Abstracts

Design considerations in a BiCMOS dual-modulus prescaler

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Design considerations in a dual modulus divide by 32/33 prescaler with a 0.6/spl mu/m BiCMOS process are presented. Care was taken to design the ECL-based circuits to operate with as low supply voltage and current consumption as possible. The phase noise contribution of the integrated bandgap bias network is demonstrated through simulations. The tradeoff between the power consumption and the phase noise is pointed out and some guidelines are provided to improve the noise performance. Measurements confirm the functionality of the prescaler with a 2.5V supply drawing around 2.3mA at 2.35 GHz with an input sensitivity between -24dBm and 12dBm. The circuit operates with a supply voltage down to 2.1V but with limited input sensitivity.

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